DARK ENERGY
SURVEY

“Light bulb” solution

Juan Estrada July 25, 2006

Light bulbs

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The light bulbs

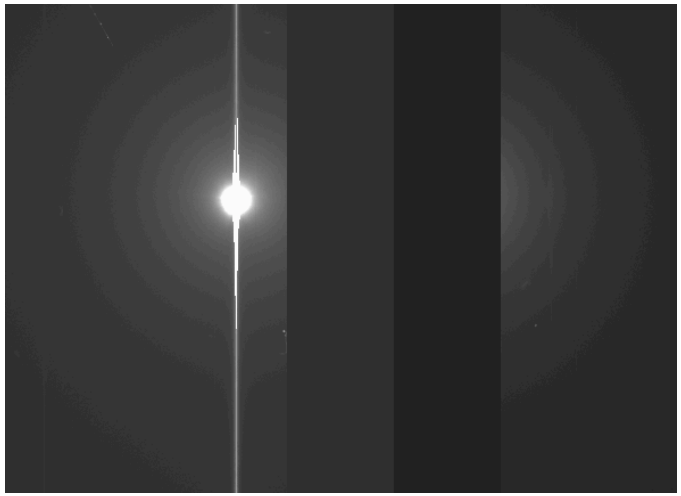
Lot 1A:

- thick = 0.6 lb/CCD
- thinned = 1.5 lb/CCD

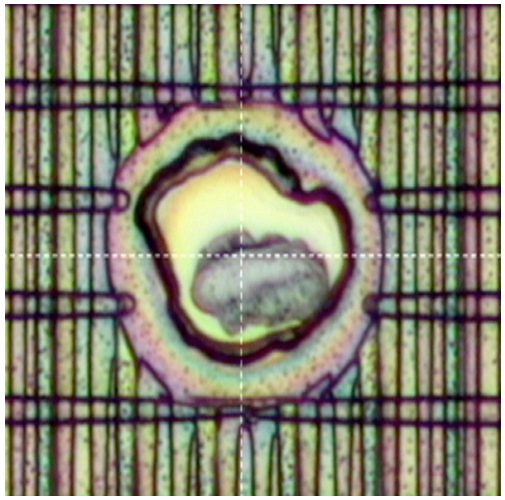
•Lot 1B:

- thick = 0.09 lb/CCD
- **thinned 1B.1: 0.4 lb/CCD**
- **thinned 1B.2: 0/8 = 0 lb/CCD (*)**

(*) LBNL process parameters optimized. Information from cold probe data (no FNAL data yet).



This makes a CCD unusable.



Background

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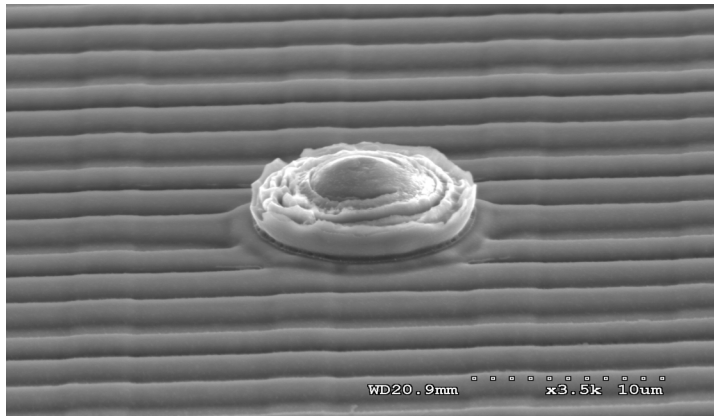
- DALSA introduced MEMs processing ~2 years ago and began using the same furnace used to deposit the in-situ doped polysilicon (ISDP) that functions as a backside gettering layer to trap defects for LBNL CCDs
- The result was a dramatic increase in large particles deposited on the front-side of the wafer, creating large defects (“lightbulbs”) and reducing yield



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Two solutions

1. Re-polish the front-side of the wafers after ISDP (current FNAL Lot 2A is in fabrication on re-polished wafers, expected back at LBNL the end of August), to arrive at FNAL in November.

   Means more steps for wafers:

   Dalsa (ISDP) -> LBNL (capping layer) -> re-polishing vendor (re-polish) -> LBNL (clean) -> Dalsa

2. Use new wafer material that already has a polysilicon backside layer (poly-backseal wafers)

   More straight forward than 1. The main question is if the poly backseal will be as effective as the ISDP (dark current). Control wafers are back and small devices give encouraging results about dark current.

Cold-probe Results on Poly Backseal Wafers compared to earlier lot with standard ISDP

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Wafer #	110253-2	110253-12	110253-24	114512-5	114512-6	114512-21
Gettering	ISDP	ISDP	ISDP	Poly Backseal	Poly Backseal	Poly backseal with early phosphorus-doping
# Hot Col Die #1	2	5	?	0	0	3
# Hot Col Die #2	1	2	3	0	0	0
# Hot Col Die #3	?	10	2	0	0	0
# Hot Col Die #4	13	5	2	0	0	0

Dramatic reduction in vertical-clock sensitive hot columns for poly backseal wafers!

Dark Current on Thick Control Poly-Backseal CCD

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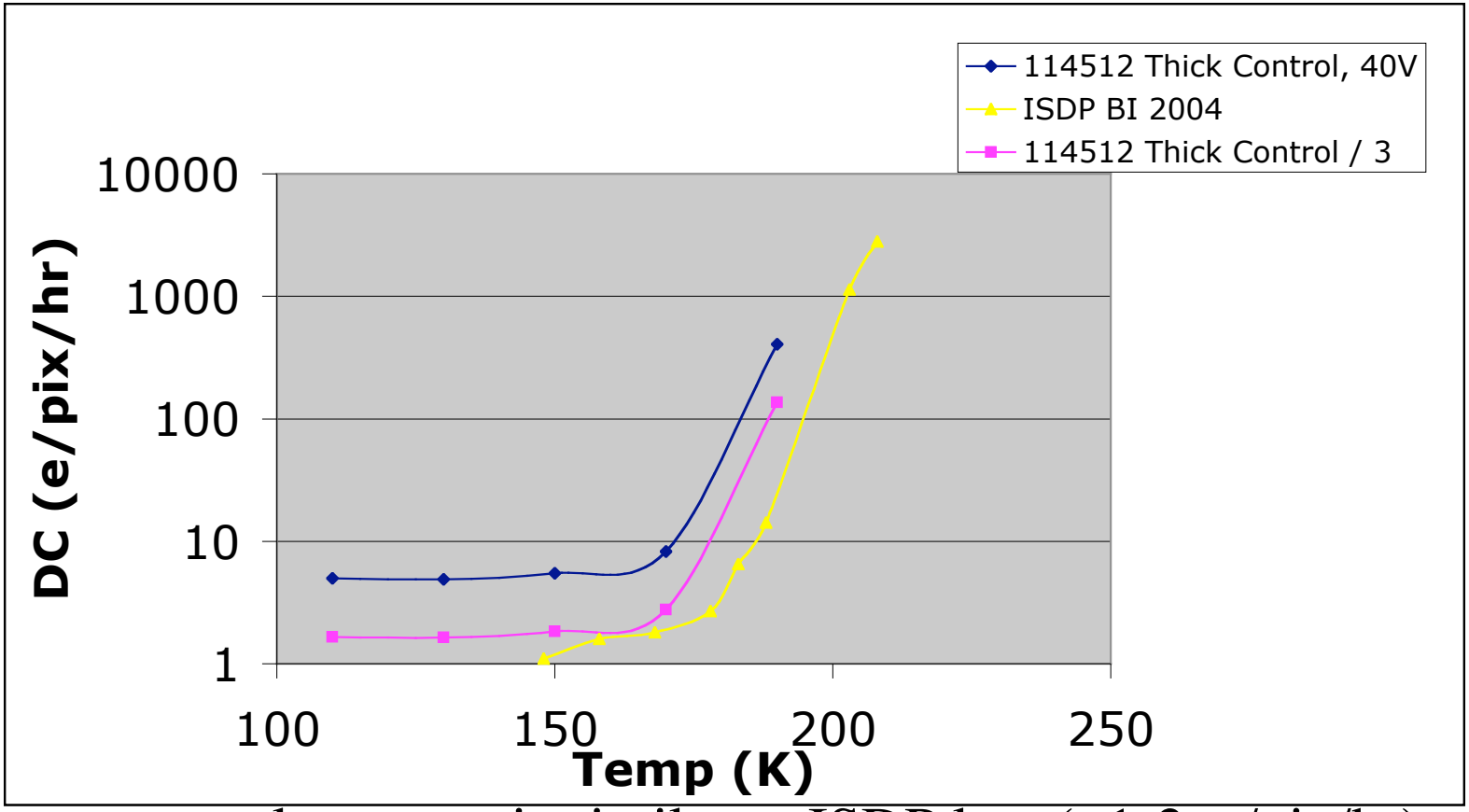

Dark current at low temp is similar to ISDP lots (~1-2 e/pix/hr) after correcting for device thickness (650 um vs 200 um)

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Backup slides

110253.23.3 - cold probe results and smart-scope scan at lightbult location

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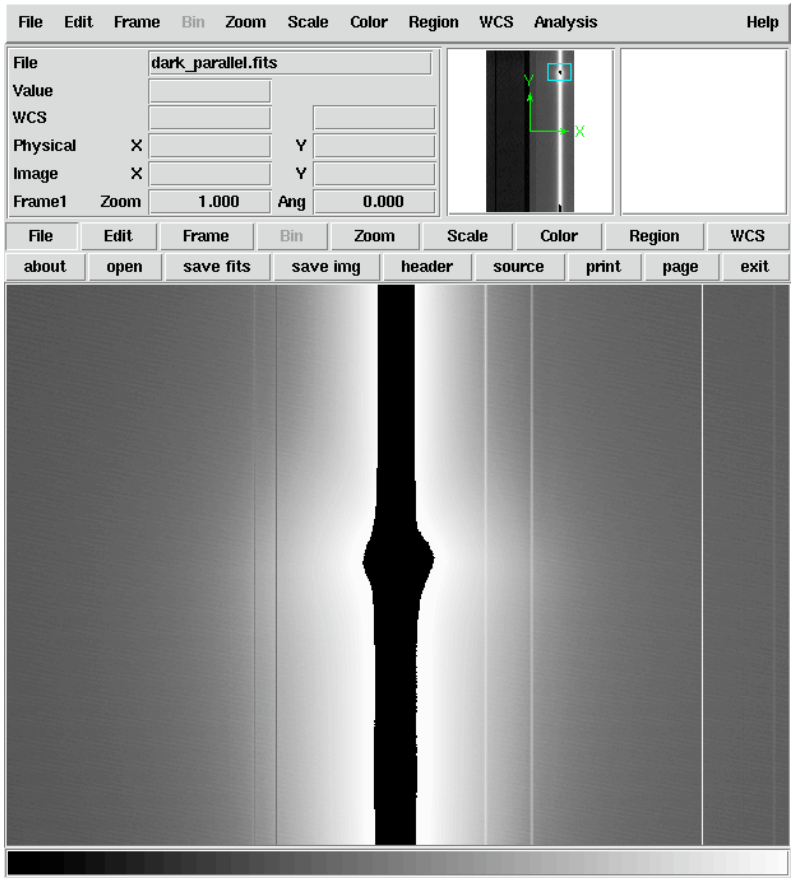

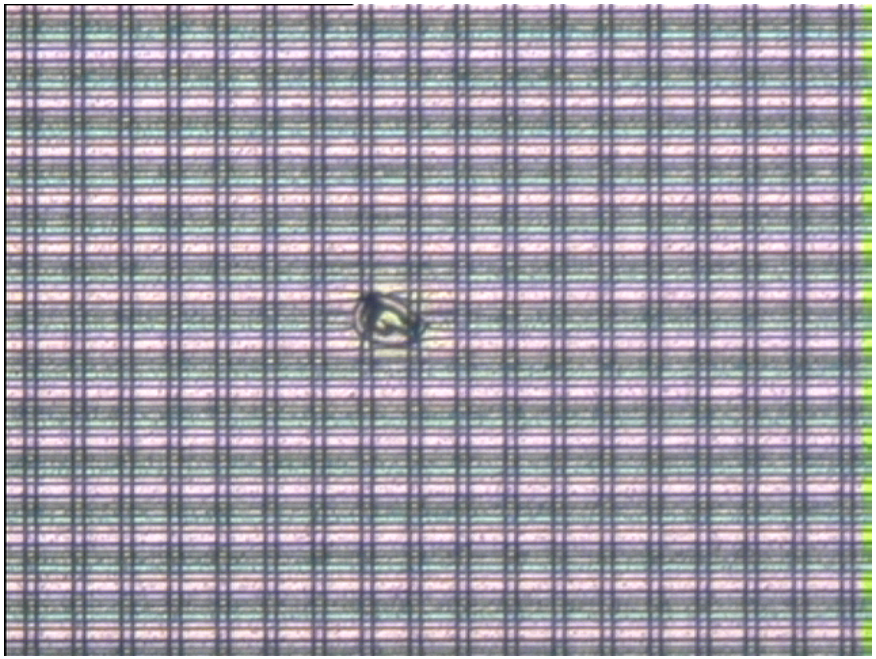

~ Centroid of defect estimated from image: X=5.75 mm, Y=56.85 mm
Smart Scope location of photograph: X=5.71 mm, Y=56.97 mm

Preliminary SEM results

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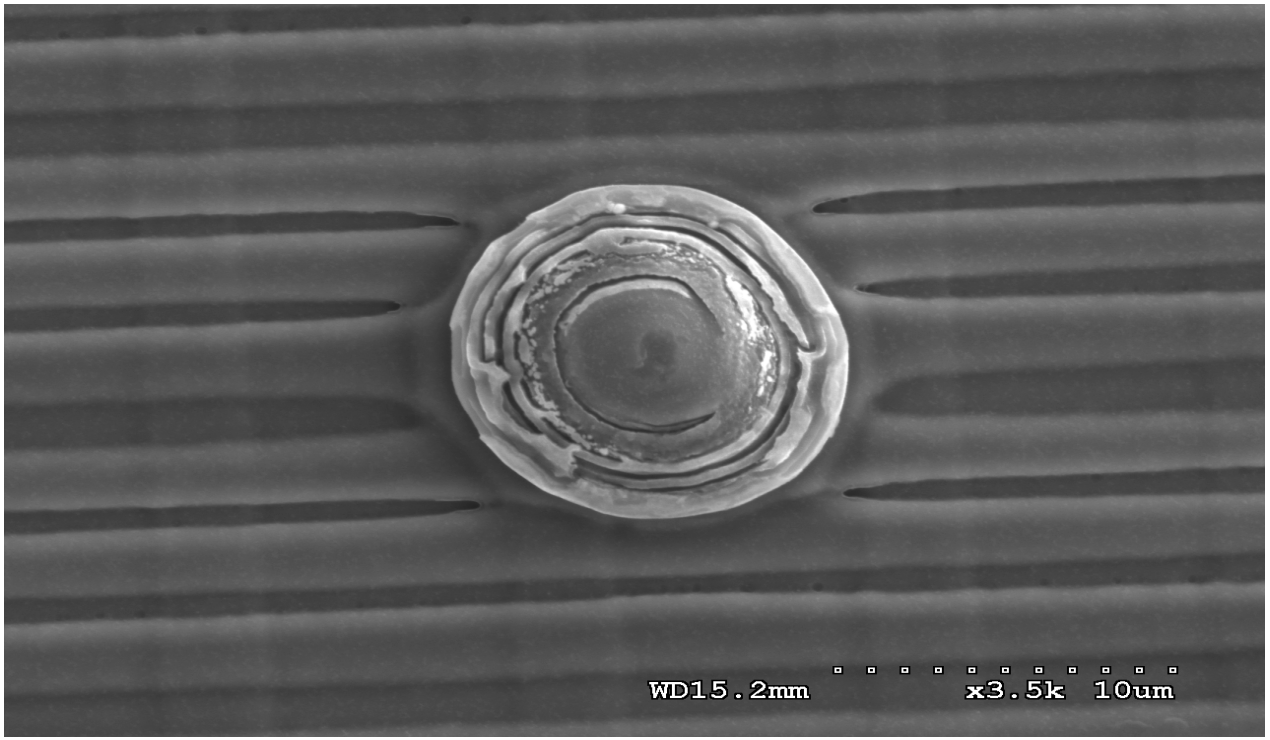

107409-21-10
Normal incidence

Fairly certain this defect corresponds to a "light bulb"
Correlation difficult with SEM coordinates (alignment of CCD to SEM not quite accurate)

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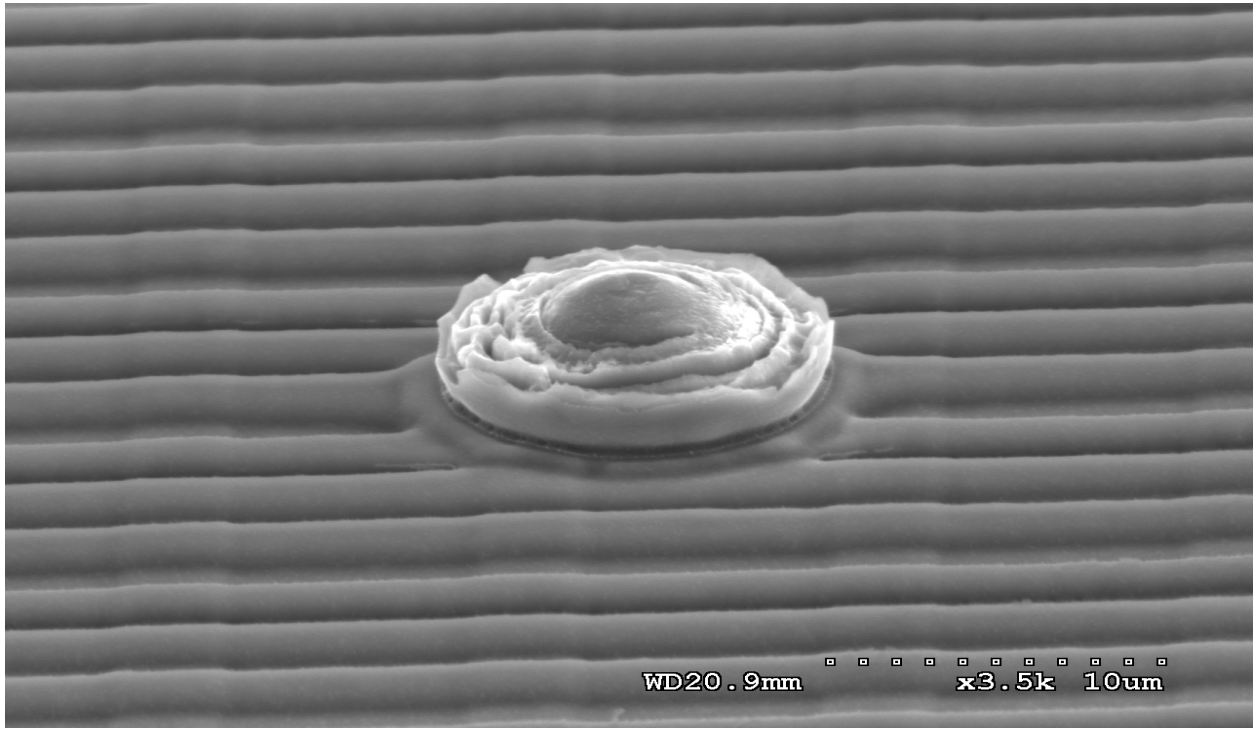
Preliminary SEM results



107490-21-10
60 degree tilt

Preliminary SEM results

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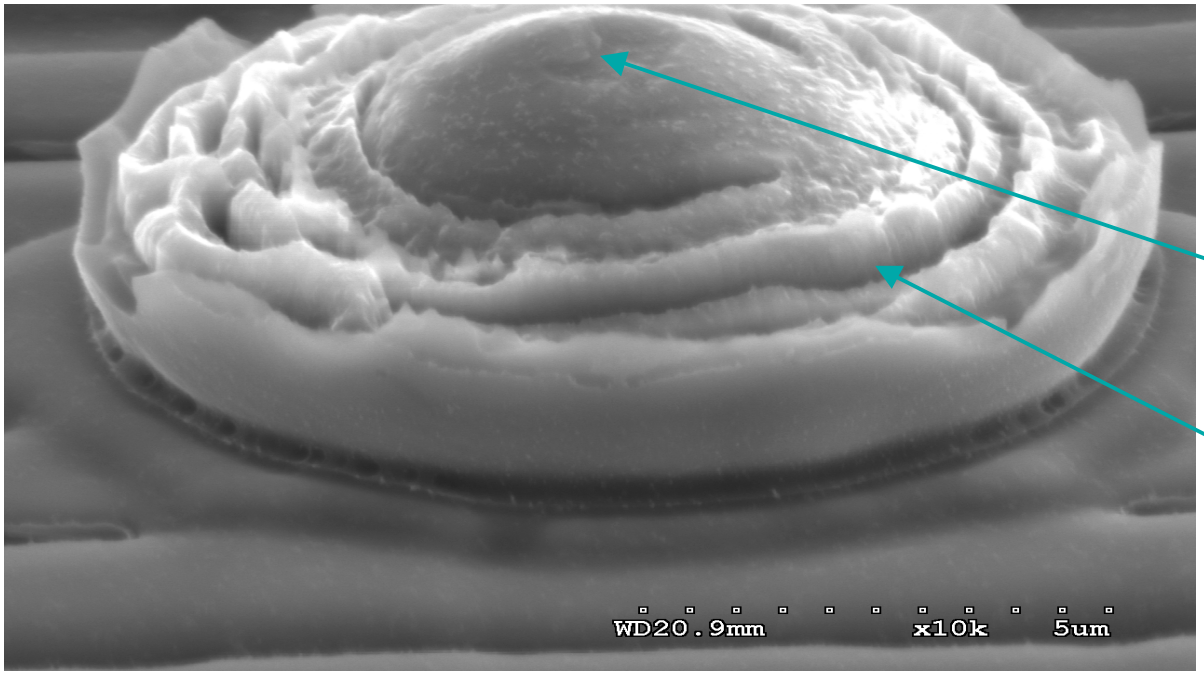

X ray fluorescence here shows Si and C (no phosphorus or O but P below detection limit)

This region shows Si, O, P (PSG)

107490-21-10
60 degree tilt

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Strategy

- After visiting DALSA in January 2006 LBNL initiated lots employing two alternate strategies:
  - re-polishing the front-side of the wafers after ISDP (current FNAL lot 2a is in fabrication on re-polished wafers, expected back at the end of August)
  - starting with a new wafer material that already has a polysilicon backside layer (poly-backseal wafers)
    - LBNL ordered 18 wafer poly backseal lot
    - 3 lot splits: no phosphorous doping, and phosphorous doping at two different stages of the processing (early and late)
    - thick control wafers are back and we have preliminary cold probe results on 2k x 4k devices
    - small test devices have been packaged and tested in dewar to measure dark curent vs temperature

Re-polished Wafers

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- Re-polishing has been done in the past at MSL and should work, but requires many extra steps:
  - DALSA deposits ISDP
  - LBNL receives wafers and deposits a silicon nitride capping layer
  - LBNL etches the accumulated front side thin films (nitride, ISDP, SiO_2)
  - LBNL sends wafers out for re-polishing to vendor
  - Re-polishing vendor measures wafers for particle counts and sizes
  - LBNL receives wafers and acid cleans them (deemed necessary after first wafer failed contaminant testing)
  - LBNL sends one wafer for destructive testing (TXRF)
  - DALSA accepts wafers for processing if TXRF results are low enough (require < 10^{10} cm^{-2} metal contamination; corresponds to < 10^{-5} of a monolayer of contaminant)

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Poly Backseal Wafers

- Poly Backseal is much more straightforward
  - DALSA buys wafers and carries out processing as usual, with one possible additional phosphorous doping step (TBD based on testing of first lot)
  - Main question is whether gettering will be as effective; determine by measuring the dark current on test lot
  - First results from test lot are encouraging